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Kuntadi Nitin Kini

2009

System-on-Chip (SoC) Design Challenges

—

Managing Non-technical Issues

by

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System-on-Chip (SoC) Design Challenges

Managing Non-technical Issues

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Dedication

This Masters report is dedicated to my dear family for providing me the strength and support to pursue this Master's program at the University of Texas, Austin.

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System-on-Chip (SoC) Design Challenges

Managing Non-technical Issues

by

Kuntadi Nitin Kini, MSE

The University of Texas at Austin, 2009

Supervisors: Bruce McCann, Tony Ambler

Efforts to increase productivity, reduce time to market, reduce costs and desire for increased functionality on a chip are driving semiconductor companies to consider SoC (System-on-a-chip) design. SoC offers the additional benefit of improving performance and design freedom. SoC designs are smaller, energy efficient and cheaper than the multi-chip solutions. Silicon manufacturing technology has improved to an extent where one can create a reliable chip with millions of transistors. Design of these complex systems, on the other hand, is taking longer and is much costlier even when the technology allows integration of the million transistor chips. Keeping these design costs low and reducing development cycle time is vital for any chip design company. Hence, companies need to delicately balance the design costs versus benefits for SoC design. Design turn-around time (TAT) even for large complex designs has been significantly improved by EDA tools despite the complexity added by the ever shrinking device geometries. However, other non technical issues and external dependencies in SoC design such as working with multi-disciplinary design teams, external IP (Intellectual Property) vendors, Electronic Design Automation (EDA) tool vendors and IP protection issues increase the risk of missing project goals and timeline. This paper will address both the technical and non-technical issues that arise when moving to SoC design and provide recommendations on how to address some of the non-technical issues involved.

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1. INTRODUCTION TO SOC DESIGN

1.1 What is SoC design?

A typical SoC design consists of multi-function units such as processor, memory, interface devices, graphics, display etc put together on the same die. Companies purchase generic processors as IP (intellectual property) and then integrate them into a SoC design.

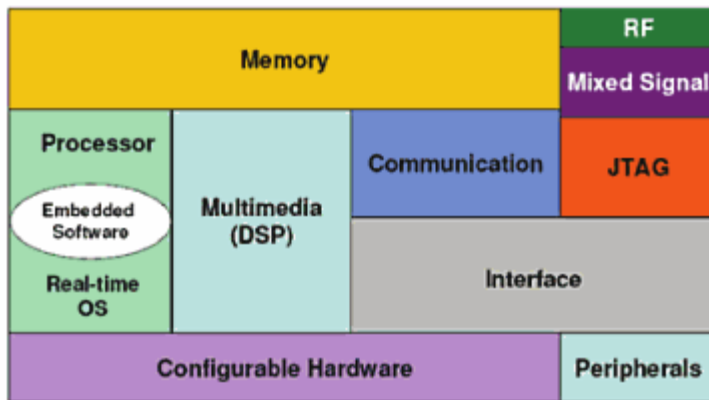


Fig. 1. A typical SoC architecture. Source: [21]

1.2 Driving forces for SoC design

SoC design is gaining acceptance in the electronics industry for the following reasons-

a) Increasing transistor density: Semiconductor technology has advanced rapidly over the past three decades allowing chip companies to integrate billions of transistors on one die as illustrated by the figure below.

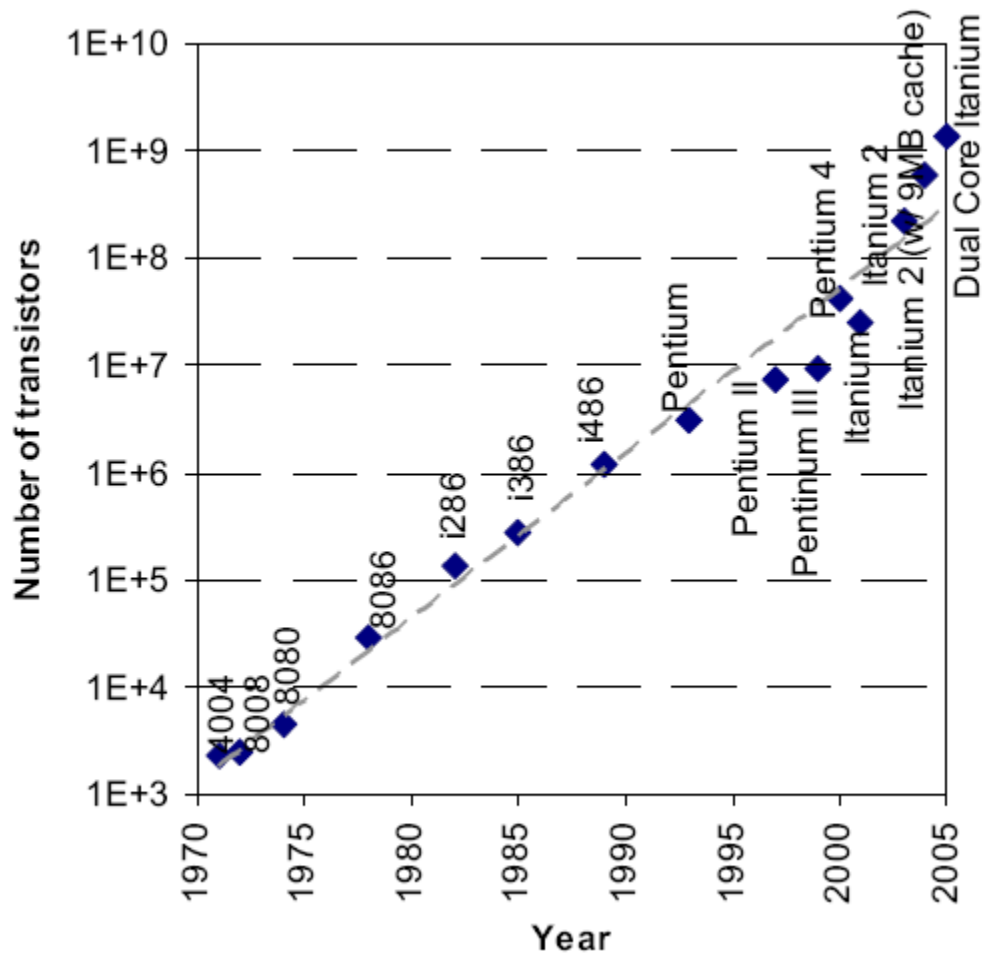


Fig. 2. Trend of increasing number of transistors per die. Source: [19]

Technology has enabled companies to take on more ambitious and complex SoC design projects

b) Flexibility: Consumers today are demanding advanced products that have the attributes of a computer, while also supporting graphics and communications. A company may have expertise in one field but not all the fields required by converged products. SoC design provides flexibility in meeting this need for varied market appliances. Today, with improvements in technology, we are seeing new SoC products ranging from iPhones,

MIDs (Mobile internet devices) and various consumer electronics such as digital television, set-top boxes and other smart appliances in today's digital home.

c) Rapid design cycles: To be competitive in current semiconductor business environment requires companies to deliver innovative products in short period of time. Technology in many ways has enabled companies to meet this goal. However, even with the latest Electronic Design Automation improvements, designer productivity has not caught up at the same rate as technology advancement in the past 20 years.

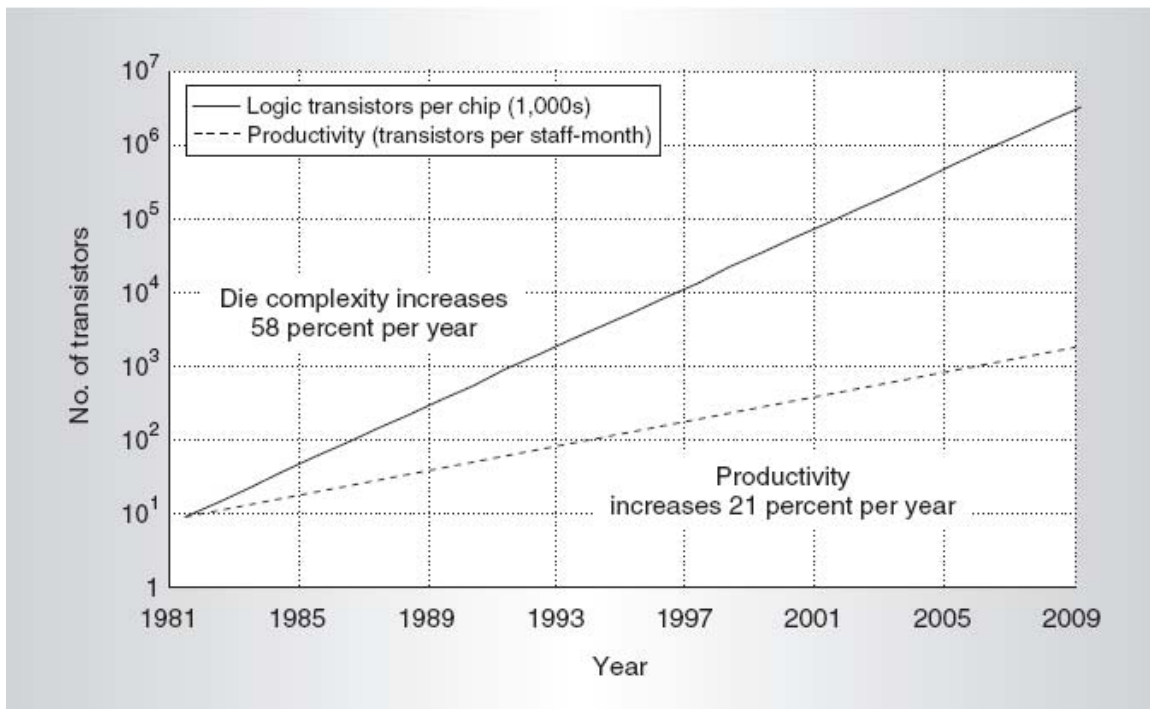


Fig. 3. Productivity gap. Source: (<http://www.sematech.org>)

One of the most effective and quickest ways to bridge this productivity gap is by reusing IP whenever possible. Rapid product design cycles can now be enabled by parallel development of IP (SoC design concept)

d) High performance products: Microprocessors started with few thousands of transistors to support basic functionality in calculators. A modern SoC, on the other hand, can have billions of transistors supporting a wide range of functions (processors/controllers, application-specific modules, data storage, and mixed-signal circuits) [19]. The need for functionality and performance is also driving companies to consider SoC design.

1.3 Future Outlook for SoC

The Gartner Market Report predicted that the \$500 million market for SoC in 2005 will grow over 80% by 2010 [20]. The annual growth rate for SoC high performance processors is estimated to be two times faster than general-purpose microprocessors [4]. The future for SoC looks bright given that there is a massive push to develop converged products and the technology to enable such large scale integration already exists

.

1.4 Market dynamics and shift in company strategy

Microprocessor companies such as Intel have predominantly focused on its core business for desktops and servers till the start of the 21st century. With introduction of Centrino microprocessor specifically targeted for mobility and low power applications, Intel expanded its horizon by targeting the mobile market-space. Market dynamics, especially in countries such as Brazil, Russia, India and China, are driving the need for mobility and smart-phones. To take advantage of this trend, traditional microprocessor companies such

as Intel, AMD are considering SoC design to bring in new exciting mobile products while trying to catch up with other well established players in the mobility market segment.

2. KEY ISSUES IN SOC DESIGN

Soc projects succeed when device integration, design and applications challenges are met. Technology has enabled device integration of billions of transistors on a single chip. Also, there are many applications that can take advantage of the SoC design capabilities. Today, the main weakness for SoC design today is the ability of design teams to integrate at system level. [19] However, there is more to SoC than just system level integration on a single die. The figure below illustrates all the key issues that influence SoC design.

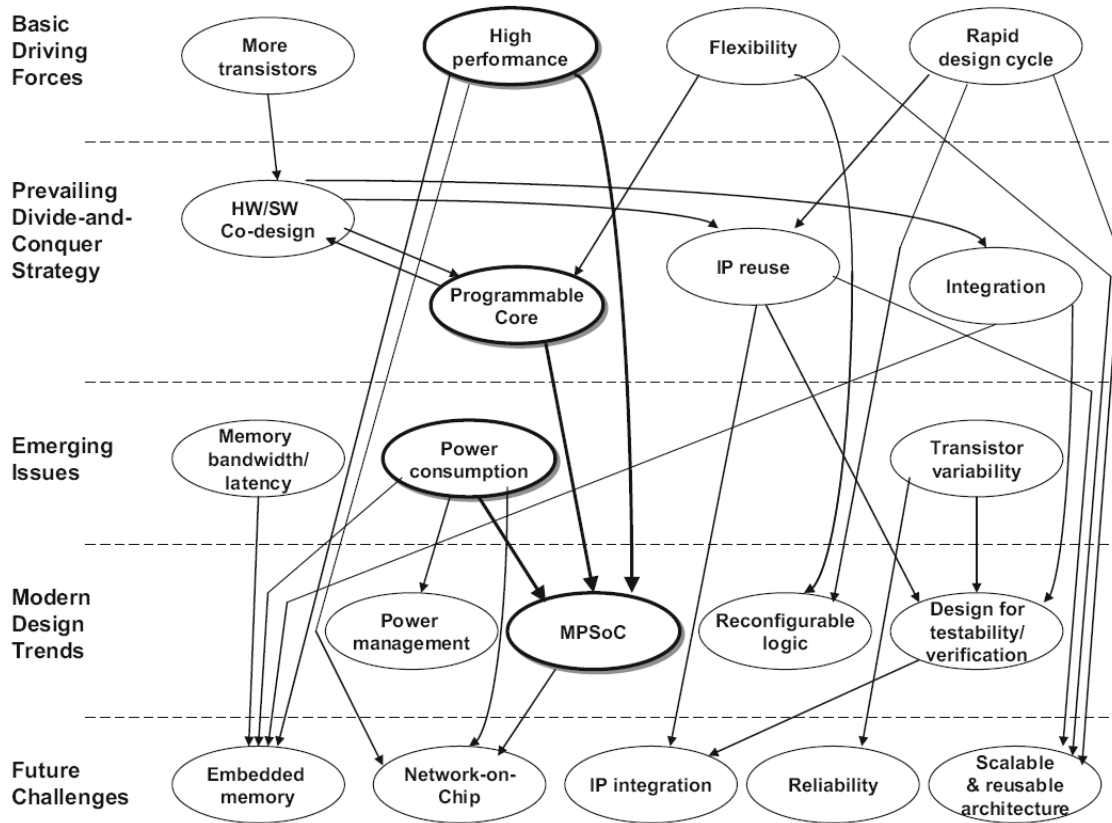


Fig. 4. The key issues in SoC design. Source: [19]

The “Basic Driving Forces” in the figure above lists several factors such as transistor density, high performance needs, flexibility and rapid design cycles which have led

companies to consider SoC design. To meet these requirements, companies are considering a “Divide-and-Conquer Strategy” which includes IP re-use for rapid design cycles, HW/SW co-design for generating programmable cores and finally integration of multiple cores and software to create various SoCs. The “Emerging Issues” are new design challenges such as Memory bandwidth, power consumption and transistor variability, which come into play especially when we integrate more transistors and memory on a single SoC. The “Emerging Issues” will need to be addressed separately using “Modern Design techniques” such as power management, multiple processor (MPSoC) designs as opposed to single processors and adding more features for testability and verification. The “Future Challenge Areas” for SoC will be in pushing the high performance limit using embedded memory and Network-on-chip strategy. Another challenge will be to reduce design TAT using enhanced IP integration strategy. SoC designs are currently trying to reuse at a higher level such as architecture level instead of just IP reuse. Furthermore, companies will also need to address reliability failures caused by transistor variability and easy migration of re-used IP from one technology to next.

2.1 Typical process of System level integration in SoC design: Currently SoC designs use the “Divide and Conquer” strategy. First, the Analog and digital domains of the SoC are carved out. The next process is to implement the carved-out domains using IP reuse, programmable cores or in-house custom design methods.

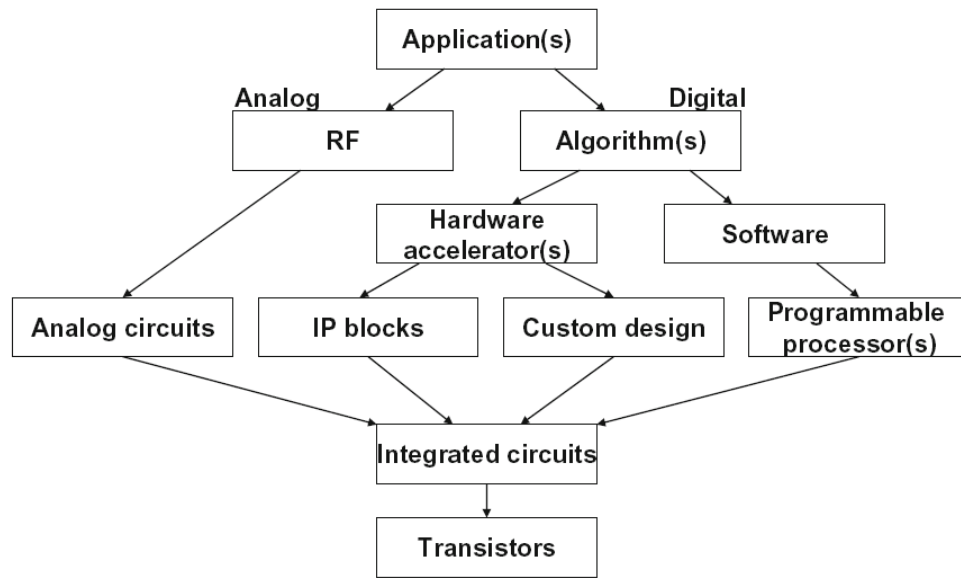


Fig.5. The divide and conquer strategy in SoC design. Source: [19]

The SoC design process also involves the cross disciplinary vertical integration of software, hardware, algorithms, applications and their interfaces (which are not shown in the figure above). Tight interaction and coordination between cross disciplinary teams is a must for successful SoC design.

2.2 Technical emerging issues that impact SoC:

SoC design faces the following important technical challenges-

a) Power consumption: The increase in power is directly proportional to the number of transistors on the chip. The power dissipation per transistor has not gone down at the same rate as the gate density increase. Also, architects are using the frequency lever to improve performance of their chips. All these factors imply that SoC design will be consuming more power than their traditional IC (Integrated Circuit) designs. Increased power consumption means increased cooling and packaging costs. Further, low power

applications need SoC designs to limit power usage in an effort to increase operating times when application is in battery powered mode. All these are compelling reasons why reducing power consumption is an important SoC design challenge.

b) Transistor variability: Beyond 20nm, we will see more variability in the behavior of transistors on the same die due to random dopant fluctuations and limitations of sub-wavelength lithography.

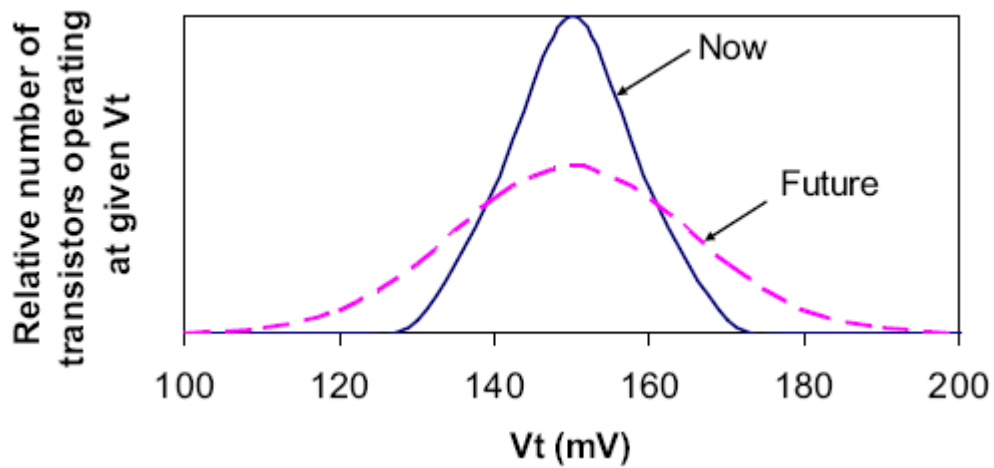


Fig.6. Variation in transistor thresholds in the future. Source: [19]

This variability will lead to unreliable circuits and hence more design and test challenges. Modeling the transistor behavior upfront and fixing manufacturing issues upfront in the design cycle is one way to reduce unreliability. Soc design architects will need to attack this challenge not only at foundry level but also through circuit design (by guard-banding for the variability effects upfront) and physical design using enhanced Design for Manufacturability techniques. New techniques will need to evolve for dealing with variability in transistor behavior below 20nm technology [19]

c) Memory bandwidth and latency: The time to access off-chip memory and DRAM (Dynamic Random Access Memory) latency have not caught up with the processor computation speed. This increasing gap between processor and memory speeds is a well-known problem, named the memory wall. [22] Also, the amount of memory integrated into an ASIC-type SoC design has increased from 20% in 1999 to 70% in 2005. [23] One of the ways to bridge the gap is to deploy as much as on-die memory using cache or local memory buffers. The improved performance from added on-die memory comes at the cost of increase in power. Hence, SoC designs will need to weigh the low power and high performance tradeoffs while trying to bridge the memory wall.

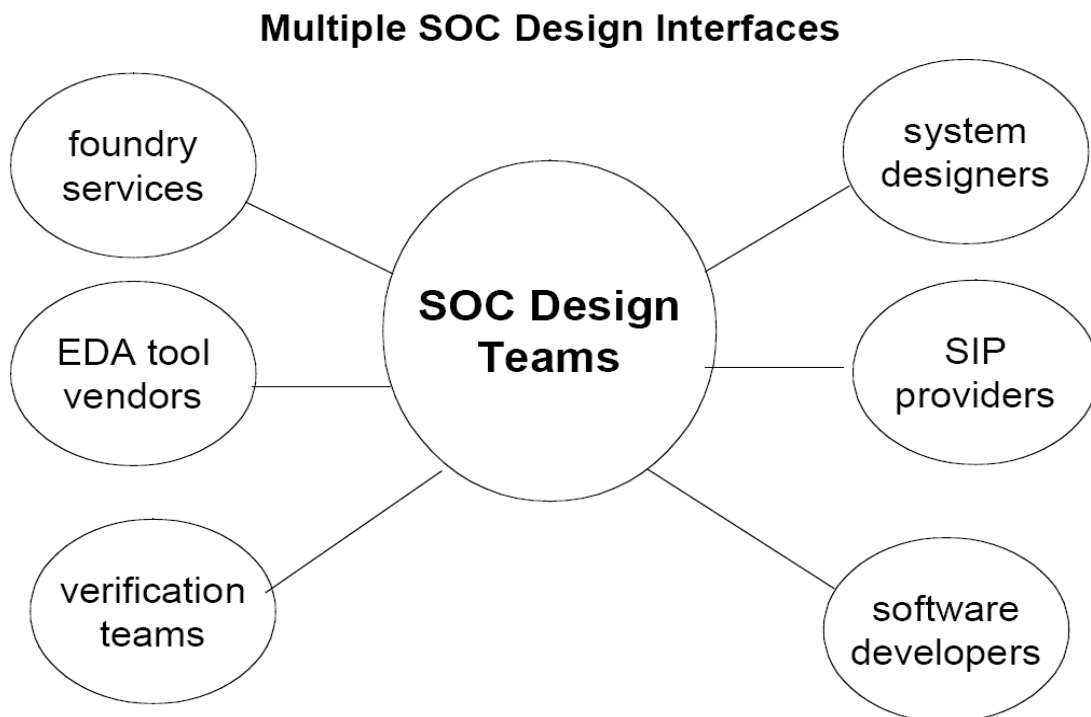
d) Design verification: A considerable amount of overall design time and resources are spent on verification aspect of SoC design. In traditional IC design, any small change in design means that it has to go through the verification process again. With the large scale integration in SoC the verification problem is further aggravated. Modular SoC design can help breakdown the verification tasks without having to re-verify the entire chip. Carefully planned test strategies which enable each IP to be tested independently from the rest of SoC design can help alleviate the verification challenge.

3. NON-TECHNICAL ISSUES FOR SOC DESIGN

The semiconductor industry has primarily focused on the technical aspects of the design, technology and IP exploration. Non-technical issues - such as work-model, organization composition, design methodology, best practices for IP selection need to be addressed for successful SOC design projects.

Design of SoC has two fundamental characteristics that set it apart from traditional IC design – sizeable design team and multi-disciplinary designs. Ambiguity and uncertainty in IPs coming from various sources further complicate the SoC project manager's task.

Multiple design interfaces:



Source: Morris, 2003

Fig. 7. Interaction of multi-disciplinary design teams that make up SoC design

SoC design imposes an organizational requirement on its design team to meet the system level challenges. Structural issues such as partitioning of design teams and communications between teams take center-stage. SoC design involves a diverse set of functional units that are integrated on a common chip. This implies that different groups that deliver the functionality need to work together and communicate effectively. There could be several groups that participate in this endeavor which may not share the common culture, tools or language with the primary design group. SoC designs using deep-submicron technologies is a good example to portray this disconnect between the design teams. A decade ago, the physical design team could be ignorant of the foundry issues and still be able to deliver a functional chip. Design teams would address the manufacturing requirements opportunistically and fix manufacturing issues only if they did not impact performance. The designer mindset and work-model has to change with technology below 45nm. Design teams have to constantly develop new techniques to address and monitor manufacturing issues. Manufacturing teams on the other hand, have to provide feedback on how the designs are performing to the DFM (design for manufacturability) metrics even before the chip tapeout. The added manufacturability requirement in the design cycle increases the TTM of the SoC design. Cross-training programs can help get the designers and manufacturing teams understand each others domain faster.

Multi-million gate ASIC (Application Specific Integrated Circuit) and SoC designs are now routinely manufactured. The new SoC challenge is to design them correctly on time and in volume with sufficient quality and reliability. Electronic Design Automation (EDA) companies are helping reduce SoC design cycles by providing flows that enable faster integration of SoC [2]. However, non-technical issues if not considered and planned upfront, can significantly delay a SoC design project. Project managers have to confront several non technical issues to enable integration of a complex SoC product. Managers have to establish communication channels between various SoC teams. They have to manage internal and external resources and make decisions on which IP to reuse and which IP to develop internally. Deciding the SoC organizational composition, enforcing IP standards, effectively managing design database, protecting IP and executing flawlessly are other factors that managers need to focus on to deliver a successful SoC product. The section below addresses each of these non-technical issues in more detail.

3.1 Communication

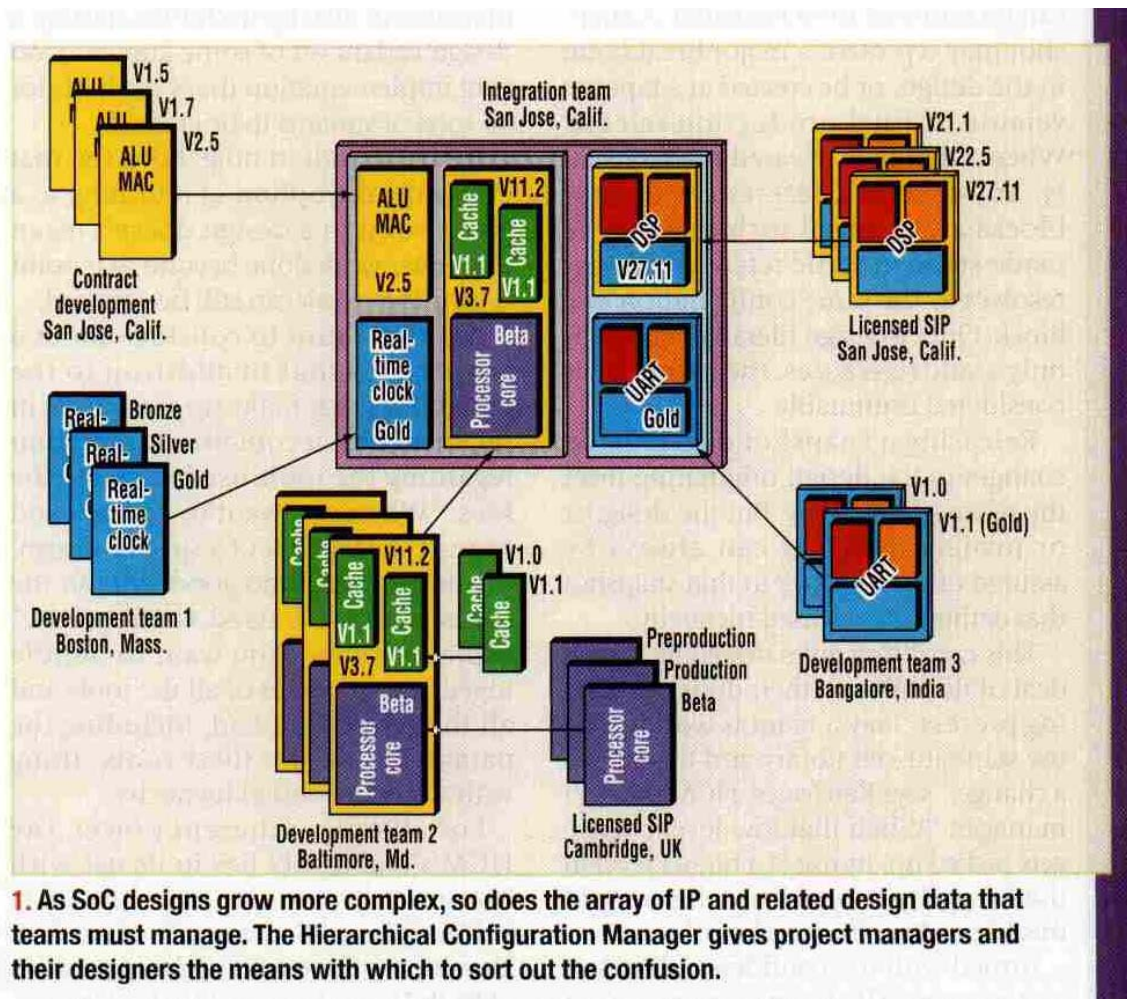


Fig. 8. The SoC design complexity- Managing the variety of IP involved. Source: [9]

As shown in the figure above, the design teams delivering SoC product maybe isolated from each other for various reasons such as geographical location, culture, goals, methodology and so on. Design teams that deliver IP which sit next to each other on the chip will communicate more than those that are far away on the chip. Such communication gaps are acceptable as long as there is no design need to communicate between teams. However, if a communication channel breaks due to personal relationships between team members then it can severely hamper the SoC design team

productivity. Fragmentation of design teams increases with the number of functional units the SoC design is divided into. Several portions of IP maybe outsourced to external IP vendors and this adds to the pre-existing isolation barrier for free flow of information. Hence, it becomes important to create formal contracts between various groups that detail how, when and what each team delivers.[11] Design teams need to agree to common protocol of how they will interact with each other for delivering IP, communicating changes in IP and format in which IP will be delivered. One of the biggest design management challenges is to keep all the different functional units coherent throughout the development cycle. Design documentation is one way to solve this problem. Design reviews should be held at major milestones or at regular intervals to sync up the various interactions that are ongoing across the SoC design. The design review meeting should include technical experts and managers to result in productive and effective meeting. The design reviews should be used as sync points to clarify goals, specifications and for tracking progress.

3.2 Managing IP risks and Communication channels: Managers should keep track not only on delivery of IP, but also ways to recreate the IP in the absence of the original design team members. Delivery of IP does not necessarily mean handing over the converged design. The responsible team should also provide detail instructions on how to reconstruct the IP. For example, when synthesized block is handed over as IP, the original design team needs to not only provide the RTL but also the synthesis directives that went into implementation of the final converged IP.

When two teams are producing IP that have no overlap and/or from a different domain of electronics discipline, communication will be heavily strained due to lack of commonality/understanding of each others design. In such a case, it would be important for SoC managers to step in and work out a framework which details what information each group delivers and breakdown of their deliverables.

Design managers need to gauge if they have enough archived information from external IP provider to deal with scenarios when the provider ceases to exist. Technical leaders should serve as a channel to track progress, answer technical questions and escalate problems to higher management in the event of schedule skips.

3.3 Organization: The drive for system level integration demands designers to have vertical skills that cover expertise of not one domain but multiple domains. Finding designers with such expertise will increase the time needed to recruit and develop good teams. Faster TAT with different people working on different designs and need for vertical system level design skill-set have a drastic impact on the SoC organizational composition. The work model for the IC designers is changing as well. Modular design approach coupled with design automation is slowly transforming the system level integration activity from a loosely organized artisan-type activity into a highly routine factory-type operation where most of the design steps are automated. [16]

3.4 Decide IP reuse and IP selection criteria: About 85% of the chips used in consumer products such as digital cellular handsets, digital cameras, personal computers, video

game devices, audio and graphics cards, and digital set-top boxes require some form of specialized functionality [6]. Companies cannot afford to develop all the required special function in-house. Typically, a project may have resources to design one specific unit or IP in-house but need to rely on external vendors to supply more established industry standard IP. Project managers have to depend on external IP for the following reasons:

- a) Out-sourcing will help their internal design resources to focus on strategic internal IP development which will help differentiate their SoC product from competition.
- b) It will help reduce design costs and risks involved by using an IP that has already proven to work.

With chip vendors rolling more and more of similar required feature set into a SoC, product differentiation is becoming increasingly difficult. Hardware implementation differences are less noticeable when more functions migrate on-chip. IP reuse does reduce time to market and help introduce a brand new product faster than competition. However, as the market matures and segments, the ability to differentiate a product offering from its competition will become increasingly critical to the success of a product. [7] Hence, managers need to be careful of how much of IP to reuse. They must also take core strengths and in-house development costs into account when deciding what portion of the IP to outsource to external vendors. Additionally, managers should use external IP which is qualified by QIP metric for quality and reuse. [6] QIP (Quality IP) is an established metric which provides information on IP attributes such as ease in integration, quality comparison with other IP vendors and IP vendor maturity &

expertise. Compatibility of the external IP, ability to mass-produce that IP, reputation of external IP vendor are all important external vendor IP selection criterion.

3.5 Enforcing Standards: The SoC design involves integration of components which are built by different IP vendors. Standards help in setting expectations and guarantee that the chip will work when the individual IP's are put together. A quote from industry expert which clearly demonstrates the need for standardization: "The OMAP 3430, one of TI's latest chip designs to tapeout illustrates the problem that design teams have. The device contains 20 million gates of logic. There are five programmable processors and "a lot of hardware accelerators", according to le Toumelin. In all, there are 70 IP cores sitting inside the chip, coming from different sites within TI and from other companies. "To put that all together and have something that works you need some standardisation," said le Toumelin." [8] Standardization of IP's will help the overall project design to converge faster.

3.6 Design data management and Documentation: It is common to see teams spread globally contributing to the SoC design. Under such circumstances, for SoC integration to work effectively requires coordination of design versions that are checked in design repository by these teams. The version of IP that needs to be used for integration from design repository will change from time to time. Integration teams will need to know which version of IP to use on a given day. Synchronicity Inc. has developed HCM (Hierarchical Configuration Manager) to manage the data for SoC projects. The tool

helps manage communication between virtual teams, versions of IP and customizations of design tools and flows. [9] HCM also allows creating immutable snapshots of the designs. This gives the design team confidence to return to or regenerate a previous good snapshot of the design while exploring new options.

Technology has allowed integration of massive numbers of transistors and functions in a SoC product. The documentation that describes the interaction between the various functional units on the chips can run into thousand of pages. Without much automation in database managements of the I/O's of these functional units, teams will find it increasingly difficult to integrate the different units of the SoC. [8]

3.7 Design methodology: Design methodology is defined as a sequence of steps by which a design process will reliably produce a design to meet the design specification, while honoring the design rules and constraints. [16] Below is an example of typical ASIC/SoC design methodology

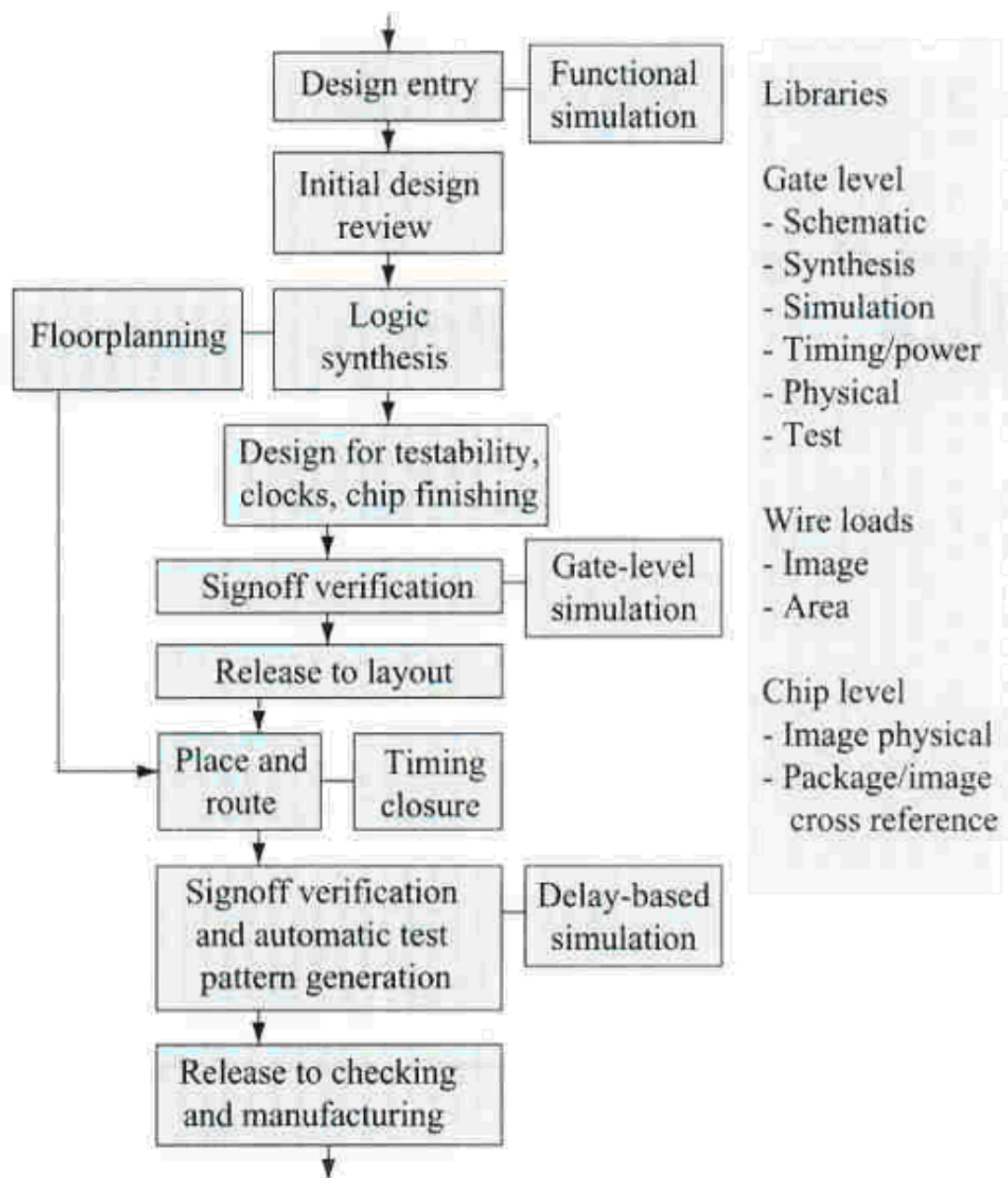


Fig. 9. Depicting a typical ASIC/SoC design methodology. Source: [2]

The figure above depicts a typical SoC/ASIC design methodology. In the initial design phase, logic designers provide the RTL (Register Transfer Language) code. The RTL

code describes the logic for a specific unit which is later converted to gate level design using EDA tools such as Synopsys Design Compiler. The technology mapped gate level netlist is then placed in the physical area on the die that is allocated to the design. This is followed by Clock tree synthesis and DFT logic insertion. Finally the design is routed and optimization tools are run to ensure that design constraints such as timing, electrical rule violations are met. Once the design has met the checklist criteria, it is then shipped to foundry for manufacturing. Traditional IC design methodology is not suited for complex design integration tasks that aim for quick TAT (Turnaround time). A modular and automated design methodology that takes system level integration into account will serve SoC designs well.

SoC design should consider hierarchical design approach rather than the flat approach. A hierarchical/modular approach allows designers to work on designs in parallel and improve TAT. Also EDA tools run faster on smaller hierarchical designs faster and reduce TTM. With flat designs, it will be very difficult for the designers to explicitly isolate designs. Also, substantial amount of design work can be reused if designs are constructed hierarchically. [2] From a technical perspective, multiple power domains within SoC can be handled more easily as well with the hierarchical approach.

3.8 Managing Critical path in Execution phase: SoC projects require integration of various components. A delay in the arrival of one component will have a cascading impact on the integration of the SoC part. Even if any component arrives early it will not

benefit the overall SoC project timeline, if other tasks hold up the integration. Hence, it becomes important to plan for the critical path early in the project.

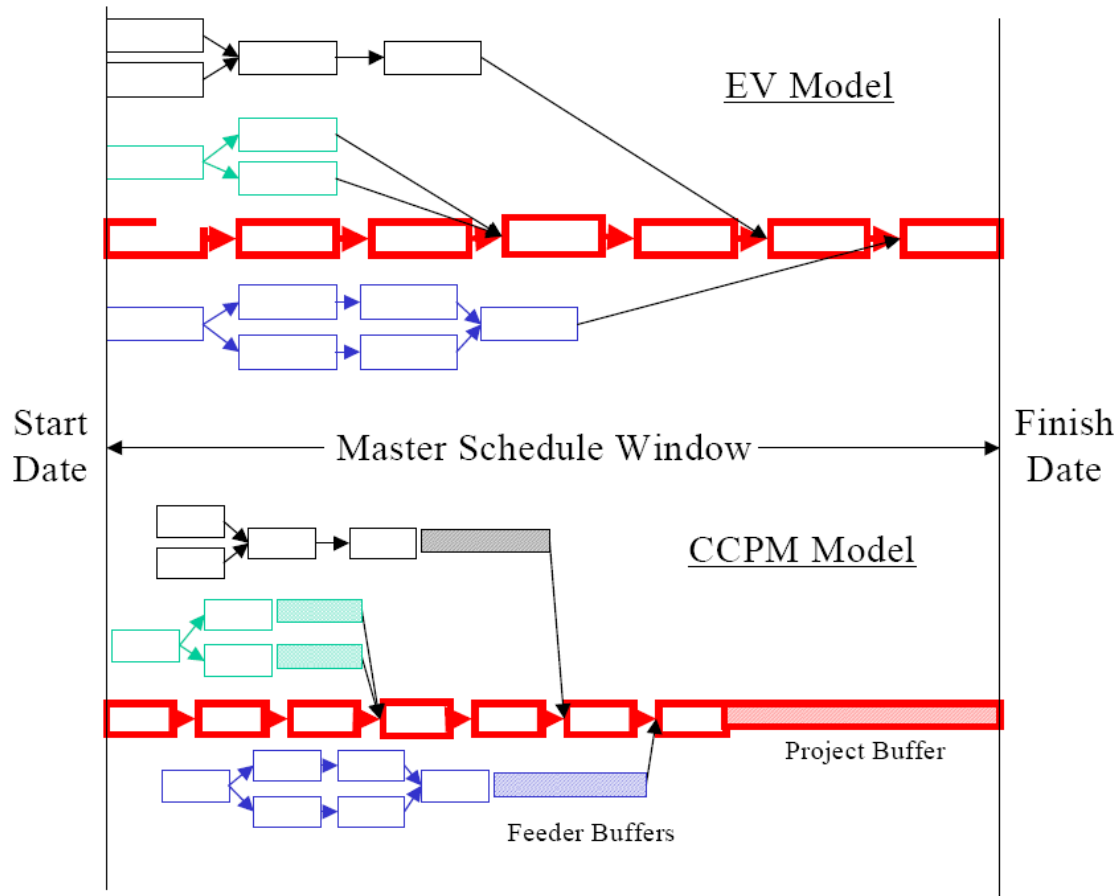


Fig 10. Critical chain Management. Source: <http://www.cnaf.navy.mil/airspeed>

All tasks that are in the critical path need to be planned aggressively. The critical path is the longest path through the project task list. By aggressively planning critical paths, project managers can create a pool of buffers. These buffers can be used to align where non-critical paths intersect the critical path. In SOC design we see such intersection of critical and non-critical paths during the integration activity. If designers in the non-critical path finish early they can help on the integration activity and thus prevent

borrowing into the critical path project buffer. Managers can then monitor the buffer usage to see if the project is tracking late or on-time. LSI Logic has used this theory of constraints (ToC) concept to simplify management of its R&D ASIC projects. [17]

3.9 IP protection: Typical microprocessor TTM (Time to market) used to be about 4 years in early 1990's but has now decreased to 18 months for more complex SOC designs. The design cycles are shrinking but on the contrary designs are getting more complex. To deliver products in a timely fashion and save design resources requires the reuse of IP from earlier pre-existing designs. The reuse of IP applies to both hardware and software IP. With widespread IP reuse, it becomes important to protect IP [18].

Software IP development is one of the critical paths in time to market for SoC design.[19] Fan YC and Shen JH have proposed a software IP release DRM (Digital Rights Management) model which can help protect vendor IP after it has been sold to the customer. Outlined below is their DRM model which captures the transactions that take place after the customer signs a contract with the Design Service/IP vendor for the software IP (which is the register transfer language). For all the transactions shown in the figure below, the IP vendor can track, authorize and release their encrypted IP using the LAN card number [18]. Throughout the different stages of the design, customer activities such as gate level synthesis, physical implementation etc are monitored and tracked by the IP vendor. The IP vendor responds to such request by enabling EDA tools to use the IP by providing a private key to decrypt the encrypted code. On completion of the physical design and post-layout verification steps the customer will send the chip to the

foundry for manufacturing. Such a DRM model protects IP, supports online ownership of IP, limits accessibility of IP to legal customers and helps monitoring IP usage.

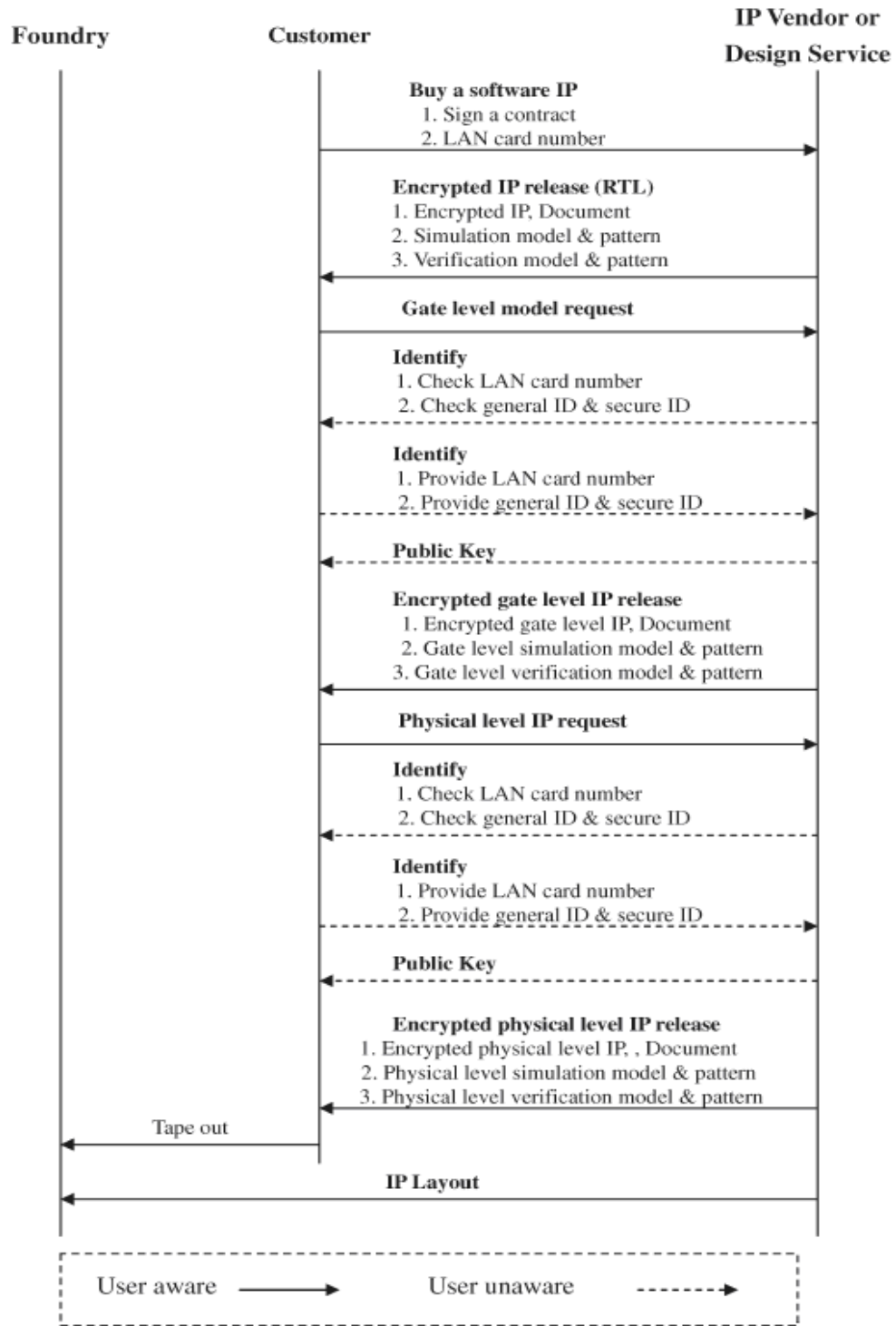


Fig. 11. IP DRM release model for an IP vendor, a user, and a foundry. Source: [18]

4. SUMMARY

SoC design is a reality today and has a bright future ahead. Market needs for high performance, reduce TAT, flexibility, large scale integration and new converged products has driven more companies to consider SoC design approach. The strengths of SoC design lies in the capability of integrating with high efficiency to generate a reliable product. This paper addressed the technical challenges such as memory bandwidth, transistor variability, power and design verification challenges that confront SoC design. There are also several non-technical issues such as communication between cross functional teams, managing risks, organizational composition and enforcing IP standards which need to be addressed.

To make a successful SoC product requires flawless design execution, selective design reuse, strong IP protection and design methodology change.

Large scale integration helps reduce TAT but also introduces new dependencies between different IPs on the SoC product. Such large scale integration involves sizable design teams both internal and external to the company and it is paramount to execute flawlessly. Flawless execution is possible when dependencies between design teams are clearly specified. SoC integration teams should clearly communicate the IP standards, IP delivery and schedule. Contracts with external vendors should be clear and detailed enough to avoid confusion.

SoC designs can reduce risks and produce reliable products by reusing as much as IP as possible. Reuse of IP can help companies cut costs and focus on key in-house IP

development. Companies should differentiate their SoC product from competition by investing in IP development where they already have competitive advantage.

SoC product gets IP from both internal design teams and external vendors.

Companies will now share the burden of protecting IP from external sources. Further, an IP leak will diminish the competitive edge of the product. Following strategies such as the DRM model for IP protection could alleviate some of the IP protection challenges.

Design methodology will need to address performance, die size and power earlier in the front-end design phase to reduce risk to schedule [2]. “Early prototyping at the RTL level offers a means to verify that new blocks operate as expected and work properly with SIP on new SoCs – heading off costly problems and saving substantially on time to market” [5]. Design automation using industry standard tools with established file interchange protocols will help SoC designs converge faster

SoC products such as cellphones present both hardware and software integration challenges. Companies that can deliver on both these fronts can bring such products to market faster.

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